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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,358	09/15/2000	Taiji Noda	0819-0423	1724

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EXAMINER	
MAI, ANH D	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ST

Office Action Summary	Application No.	Applicant(s)	
	09/662,358	NODA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 08 August 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12,15,21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10,12,15,21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 8, 2005 has been entered.

Status of the Claims

2. Amendment filed August 8, 2005 has been entered. Claim 6 has been amended. Claims 1-10, 12, 15, 21, 23 and 24 are pending. Non-elected invention, claims 1-5 have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-10, 12, 21, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr et al. (U.S. Patent No. 5,650,340), in view of Richards, Jr. et al. (U.S. Patent No. 5,786,620) and Sultan (U.S. Patent No. 5,970,353) (all of record).

With respect to claim 6, Burr teaches a method for fabricating a semiconductor device substantially as claimed including:

a first step of forming a gate electrode (125) over a semiconductor region (121) with a gate insulating film (123) interposed therebetween; (see Fig. 4F);

a second step of implanting heavy ions into the semiconductor region (121) on the side of the gate electrode (125) using the gate electrode (125) as a mask, thereby forming a first ion implanted layer (116) of a second conductivity (p), at least upper part of which is an amorphous layer, wherein the heavy ions are indium ions at a dose of 5E12 to 5E13 cm^{-2}; (see Fig. 4G, col. 11, lines 57-67);

a third step of implanting ions of a first dopant (n) into the semiconductor region (121), in which the amorphous layer has been formed, using the gate electrode (125) as a mask, thereby forming a second ion implanted layer (131A-B) of a first conductivity type (n); (see Fig. 4H);

a fourth step of conducting a first annealing process to activate the first (116) and second (131A-B) implanted layers, thereby forming an extended high-concentration dopant diffused layer (131A-B) of the first conductivity type (n) though diffusion of the first dopant (n) and a pocket dopant diffused layer (116) of the second conductivity type (p), which is in contact with a bottom portion of the extended high-concentration dopant diffused layer (131A-B), through diffusion of the heavy ions (B, In), respectively,

wherein in the second step, a dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ions implantation, and

in the fourth step, the pocket dopant diffused layer (116) is formed having a peak dopant concentration produced by trapping heavy ions (B, In) in the dislocation loop layer, the pocket dopant diffused laver (116) and the extended high-concentration dopant diffused laver (131 A-B) are in contact at the peak dopant concentration of the pocket dopant diffused laver (116) and a

side of the extended high-concentration dopant diffused laver (131A-B) located below the gate electrode is not covered by the pocket dopant diffused laver (116). (See Fig. 4F-I, col. 10, line 45-col. 12, line 44).

Thus, Burr is shown to teach all the features of the claim with the exception of implanting heavy ions into the semiconductor region (121) on both sides of the gate electrode (125) and the dose for the indium heavy ions to be about $1x10^{14}$ to $1x10^{16}$ /cm^2.

Note that the claimed dose of about $1x10^{14}$ to $1x10^{16}$ /cm^2 does not appear to be critical.

However, Richards teaches that to reduce the short channel effects (SCE) both source and drain pocket implants are preferably used to simplify the process. (See col. 21, ll. 46-56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to implant heavy ions into the semiconductor region of Burr on both sides of the gate electrode as taught by Richards to simplify the process.

Further, Sultan teaches that a higher indium ions dose $1x10^{14}$ /cm^2 have been used to amorphize and to form pocket dopant diffusion layer (62). (See col. 6, lines 6-20).

Note that the specification contains <u>no disclosure</u> of either the *critical nature of the claimed* dose of about $1x10^{14}$ to $1x10^{16}$ /cm^2 of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Moreover, Applicants has freely admitted that "if the ions are implanted at an implant dose of $5x10^{13}$ /cm^2 or more, then the

amorphous layer can be formed inside the semiconductor substrate 100". (page 19, line 23-page 20, line 2). Thus, the claimed range is not critical.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to implant indium heavy ions of Burr at the dose as taught by Sultan to amorphize and form pocket dopant diffusion layer.

With respect to the limitation "at least upper part of which is an amorphous layer", the upper part of the semiconductor region (121) is amorphized by the implantation of the heavy ions that form the first ion implanted layer (116). This is well known in the art.

With respect to the functional limitation "the pocket dopant diffused layer is formed having a peak dopant concentration produced by trapping heavy ions in the dislocation loop layer", this is an inherent result of the implantation of heavy ions, such as indium, into the semiconductor region.

With respect to claim 7, the part of the pocket dopant diffused layer (116) of Burr in which the heavy ions (In) are trapped should overlap with a dopant profile of the extended high-concentration dopant diffused layer (131A-B). (See Fig. 4H).

With respect to claim 8, method of Burr further includes:

forming a sidewall spacer (135) on side faces of the gate electrode (125) after the third step has been performed;

implanting ions of a second dopant (n) into the semiconductor region (121) using the gate electrode (125) and the sidewall spacer (135) as a mask, thereby forming a third ion implanted layer (137A-B) of the first conductivity type (n); and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer (137A-B) of the first conductivity type (n), which is located outside of the extended high-concentration dopant diffused layer (131A-B), has a junction deeper than that of the extended high-concentration dopant diffused layer (131A-B) and has been formed through diffusion of a second dopant. (See Fig. 4I).

With respect to claim 9, the heavy ions of Burr are implanted at such an implant energy as forming an amorphous/crystalline interface, through implantation of the heavy ions, at a level equal to or deeper than a range of the first dopant (n^-) and shallower than a range of the second dopant (n^+).

With respect to claim 10, method of Burr further includes:

implanting ions (p) into a surface part of the semiconductor region (111), thereby forming a fourth ion implanted layer (121) of a second conductivity type (p) before the first step is performed; and

conducting a third annealing process to activate the fourth ion implanted layer (p), thereby forming a dopant diffused layer (121) to be a channel region. (See Fig. 4B, col. 10, line 64-col. 11, line 13).

With respect to claim 12, the heavy ions of Burr are implanted at such an implant energy (50-70 KeV) as making the range of the heavy ions equal to or deeper than the range (20-60 KeV) of the first dopant (131A-B) and between one to three times as deep as the range of the first dopant (131A-B).

With respect to claim 21, the first dopant of Burr is arsenic.

With respect to claim 23, the first and second dopant of Burr are arsenic.

With respect to claim 24, the fourth ion implanted layer (121) of Burr is formed into the surface part of the semiconductor region (111) by implanting p-type dopant.

Thus, Burr is shown to teach all the features of the claim with the exception of explicitly disclosing p-type dopant includes indium.

However, boron and indium are well known in the art as p-type dopants in silicon system and subsequently used to form p-type layer 116.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form layer 121 of Burr using indium ions because either boron or indium ions are well known p-type dopant.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr '340, Richards '620 and Sultan '353 as applied to claim 6 above, and further in view of Tsukamoto (U.S. Patent No. 5,399,506) of record.

Burr and Richards teach conducting the first annealing process using a rapid thermal annealing (RTA) as is well known to those skill in the art.

Thus, Burr and Richard are shown to teach all the features of the claim with the exception of explicitly disclosing the details of RTA process.

However, Tsukamoto teaches that RTA process is well known in the art including: a semiconductor region is heated up to a temperature between 950 °C and 1050 °C at a rate between 100 °C/sec to 150 °C/sec and then kept at the temperature for a period of time between 1 to 10 seconds.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention perform the RTA process of Burr as taught by Tsukamoto to activate the dopants.

Response to Arguments

5. Applicant's arguments filed February 15, 2004 have been fully considered but they are not persuasive.

With respect to the dose of indium ions, there is no criticality regarding the claimed doses. Applicant has freely admitted that at the dose of $5x10^{13}$ /cm^2, the semiconductor substrate 100 is amorphized in the same fashion as at the higher doses (about $1x10^{14}$ to $1x10^{16}$ /cm^2).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Note that, Richards is cited to show symmetry implanted (both sides of the gate) is routinely performed by skill worker in the art. Sultan, on the other hand, is cited to show the amorphize dose as claimed ($1x10^{14}$ /cm^2) is well known.

Thus, the combination of the references has rendered the claims obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER